H1392

ENGINEERED METAL GATE ELECTRODE

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TECHNICAL FIELD

[01] The present invention relates to semiconductor devices comprising transistors with metal gate electrodes and to fabrication techniques for engineering a metal gate electrode with a tunable work function and high quality gate dielectric. The present invention is particularly applicable to fabricaturing high speed semiconductor devices having submicron design features.

BACKGROUND ART

[02] The integration of hundreds of millions of circuit elements, such as transistors, on a single integrated circuit necessitates further dramatic scaling down or micro-miniaturization of the physical dimensions of circuit elements, including interconnection structures. Micro-miniaturization has engendered a dramatic increase in transistor engineering complexity, such as the inclusion of graded well-doping, epitaxial wafers, halo implants, tip implants, lightly doped drain structures, multiple implants for source/drain regions, silicidation of gates and source/drains, and multiple sidewall spacers, for example.

[03] The drive for high performance requires high speed operation of microelectronic components requiring high drive currents in addition to low leakage, i.e., low off-state current, to reduce power consumption. Typically, the structural and doping parameters tending to provide a desired increase in drive current adversely impact leakage current.

[04] Recently, metal gate electrodes have evolved for improving the drive current by reducing polysilicon depletion. However, simply replacing polysilicon gate electrodes with metal gate electrodes may engender issues such as, increased leakage current because of an undesired value of work function which in turn provides undesired electrical characteristics for the transistor. The work function is the amount of energy required to excite electrons across a threshold. Polysilicon gates on silicon substrate provide a work function that allows the gates to be adequately controlled. However, the use of a metal gate electrode on a silicon substrate undesirably alters the work function vis-à-vis polysilicon, thereby reducing the controllability of the gate. Another disadvantage of a metal gate process resides in forming the metal gate electrode prior to high temperature annealing to activate the source/drain implants, as at a temperature in excess of 900°C. This fabrication technique may degrade the metal gate electrode or cause interaction with the gate dielectric, thereby adversely impacting transistor performance.